REMARKS/ARGUMENTS

In the Office action dated Jul7 13, 2005, the Examiner rejected claims 1-13, all of the claims in the Application under 35 U.S. C. § 102(e) as being anticipated by U.S. Patent No. 6,562,703 B1 of Maa *et al.*. The Examiner also rejected claims 1-13 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,464,780 B1 to Mantl *et al.*

In the Specification, no changes.

In the Claims, claims 1, 6 and 9, all of the independent claims, are currently amended.

The Invention

The method of the invention produces a thick, *e.g.*, 100 nm to 500 nm, relaxed, smooth SiGe film having a high Ge content, *e.g.*, greater than about 20% to 30% or more, as a buffer layer for a tensile strained silicon film, which is suitable for use in high speed MOSFET applications. It is critical that the top portion of this SiGe film be as defect-free as possible in order to minimize leakage currents and to maximize carrier mobilities and device yield. To accomplish this, the dislocations which relax the SiGe film must be confined as much as possible to the region close to the SiGe/silicon substrate interface. This is partly accomplished by having a very high density of dislocations nucleated at this interface, which in turn is due to the strain caused by defects resulting from hydrogen implantation and annealing. The order of performing the steps of the method of the invention are set forth in Fig. 1 of the Application, and include, *seriatim*, preparing a silicon substrate; deposition a layer of SiGe, which will ultimately become a relaxed SiGe buffer layer; implanting ions through the SiGe into the silicon substrate; annealing the structure; and depositing a layer of tensile-strained silicon on the now-relaxed SiGe buffer

layer.

The Applied Art

U.S. Patent No. 6,562,703 B1, granted May 13, 2003, to the inventors of the instant Application, describes a similar, but not anticipatory method of invention, which includes preparing a silicon substrate; forming a silicon buffer layer thereon; depositing a SiGe layer on the silicon buffer layer; implanting ions through the SiGe and silicon buffer layers into the silicon substrate; annealing; and depositing a tensile-strained silicon layer on the now relaxed SiGe layer.

U.S. Patent No. 6,464,780 B1, granted October 15, 2002, to Mantl *et al.*, describes a method of fabricating a substrate beginning with a silicon wafer; implanting ions into the silicon wafer; depositing a layer of SiGe on the ion-implanted wafer, and annealing. Alternately, the ion implant and SiGe deposition may be reversed.

The Claims

Claims 1, 6 and 9 have been amended to recite that the steps therein must be performed *seriatim*. This limitation is supported by the flow chart of Fig. 1. The claims have also been amended to include a limitation that the final anneal forms a relaxed SiGe buffer layer, which is supported by the disclosure in the Specification, page 5, lines 6 - 14. Perhaps the best way to distinguish Applicants' claims from the applied art is with the following table, which sets forth salient limitations of Applicants' amended claim1 and the two applied references:

Claim 1	6,562,703 B1 35 U.S. C. § 102(e)	6,464,780 B1 35 U.S.C. § 103(a)
Prepare silicon substrate	Prepare silicon substrate	Prepare silicon substrate
		(a) Implant H ions
Deposit SiGe layer - which will become SiGe buffer layer	Deposit silicon buffer layer	(a & b) Deposit SiGe layer
	Deposit SiGe layer	
	Deposit oxide layer	
Implant H ions	Implant H ions	(b) implant H ions
	Remove oxide layer	
Anneal	Anneal	Anneal
Deposit tensile-strained silicon	Deposit silicon layer	Not specified

It is clear that '703 is not a proper 35 U.S. C. § 102(e) reference - because it requires deposition of a silicon layer before deposition of a SiGe layer, and requires deposition and removal of an oxide layer. Applicants' claims do not require that a silicon buffer layer be deposited, nor do they require that an oxide layer be deposited and removed. Thus, in order to say that '703 anticipates Applicants' claims, two critical steps of the method of the invention of '703 must be omitted - rendering the method of the invention of '703 inoperable, thereby destroying the utility of the invention. Likewise, '780 does not provide a SiGe buffer layer in either its (a)(Example 1) or (b)(Example 2) technique. Neither does '780 suggest that the method of the invention be practiced in a given order of steps. Claim 1 is therefore allowable over the applied art.

Claims 2-5 are allowable with their allowable parent claim.

Claim 6 is allowable for the reasons set forth in connection with claim 1.

Claims 7 and 8 are allowable with their allowable parent claim.

Claim 9 is allowable for the reasons set forth in connection with claim 1.

Claims 10 - 13 are allowable with their allowable parent claim.

In light of the foregoing amendment and remarks, the Examiner is respectfully requested to reconsider the rejections and objections stated in the Office action, and pass the application to allowance. If the Examiner has any questions regarding the amendment or remarks, the Examiner is invited to contact the undersigned.

Provisional Request for Extension of time in Which to Respond

Should this response be deemed to be untimely, Applicants hereby request an extension of time under 37 C.F.R. § 1.136. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any over-payment to Account No. 22-0258

Customer Number

55376

Respectfully Submitted,

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